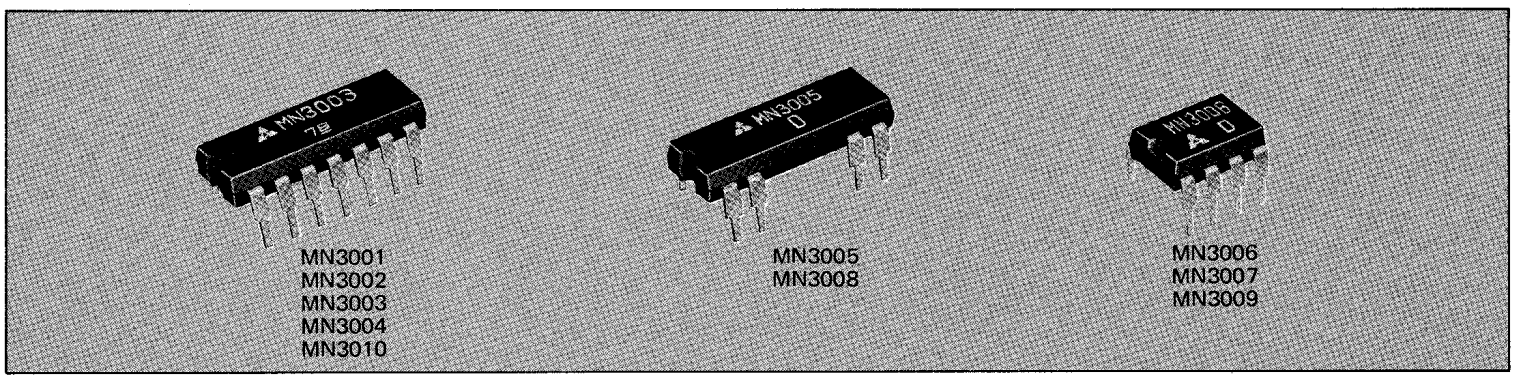
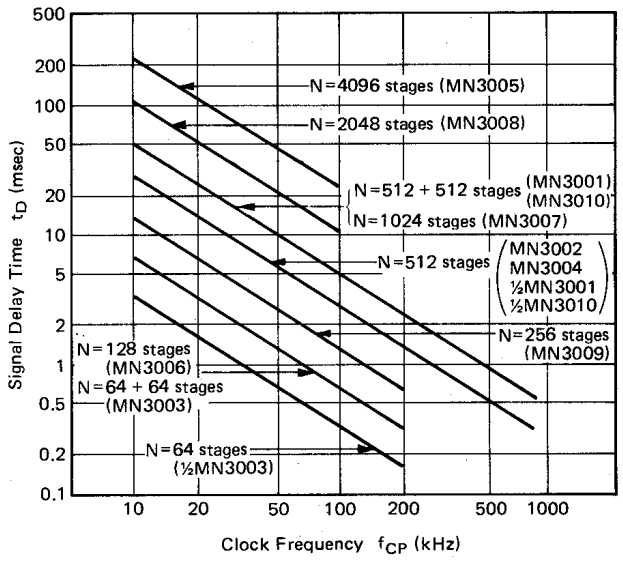
BBD's for variable delay lines in audio frequency range.



- P-channel silicon gate; tetrode MOS transistors configuration
- Signal delay: 6.4 msec to 204.8 msec
- Clock frequency range: 10 ~ 200 kHz
- Signal to noise ratio: 70dB ~ 90dB (typ.)
- Low distortion

t_D–f_{CP}



Stage		Type No.	Noise	Application
64	Dual Type	MN3003	Low Noise Types	Reverberation Effect (Signal Delay under 10 msec) Vibrato Effect *1 Chorus Effect *2 Phasor/Flanger Effect *3
128	Single Type	MN3006		
256		MN3009		
512		MN3004		
		MN3002	Standard Types	Echo Effect (Signal Delay over 10 msec.) Double Voicing Effect *4
	Dual Type	MN3001		
		MN3010	Low Noise Types	
1024	Single Type	MN3007		
2048		MN3008		Reverberation Effect (Signal Delay over 100 msec.)
4096		MN3005		

*1 Vibrato Effect: Several H_Z moduration effect of the clock frequency for BBD.
*2 Chorus Effect: Mixing effect of the original signal and the attenuated delayed signal.
*3 Phasor/Flanger Effect: Effect of either the sum or difference of the original signal and the delayed signal.
*4 Double Voicing Effect: Mixing effect of the original signal and the delayed signal.

△ Preliminary

	Item	Symbol	MN3001	MN3002	MN3003	MN3004	MN3005	MN3006	△ MN3007	△ MN3008	△ MN3009	△ MN3010	Unit
Circuit Construction	Number of BBD		Dual-512	512	Dual-64	512	4096	128	1024	2048	256	Dual-512	Stage
	Clock Generator		External		Built-in	External							
	Output Terminal		Pair										
Operating Conditions	Drain Supply Voltage	V_{DD}	−15		−9	−15	−15	−15	−15	−15	−15	−15	V
	Gate Supply Voltage	V_{GG}	−14		−8	−14	−14	−14	−14	−14	−14	−14	V
	Back-Gate Bias Voltage	V_{BB}	+5		Not Needed								V
	Clock Voltage "H"	V_{CPH}	0		0	0	0 ~ −1	0 ~ −1	0 ~ −1	0 ~ −1	0 ~ −1	0 ~ −1	V
	Clock Voltage "L"	V_{CPL}	−15		−9	−15	−15	−15	−15	−15	−15	−15	V
	Input DC Bias	V_{bias}	−3.3 ~ −4.9		−2.5~−6	−5~−10	−5~−10	−5~−10	−5~−10	−5~−10	−5~−10	−5~−10	V
Electrical Characteristics	Input Signal Frequency (fcp = 40kHz, 3dB down)	f_i	12				10	12			14	12	kHz (max.)
	Input Signal Swing	V_i	1.8		0.8	1.8	1.2	1.8	1.5	1.5	1.7	1.8	Vrms(max.)
	Insertion Loss	L_i	8.5		3.5	1.5	0	0	0	0	0	0	dB (typ.)
	Total Harmonic Distortion	THD	0.4		0.5	0.4	1	0.2	0.5	0.5	0.3	0.4	% (typ.)
	Noise Level	V_N	250 (typ.)		100(typ.)	210	400	80	250	300	150	210	μV (max.)
	Signal to Noise Ratio	S/N	70		75	85	75	90	80	78	88	85	dB (typ.)
	Signal Delay Time	t_D	51.2	25.6	6.4	25.6	204.8	6.4	51.2	102.4	12.8	51.2	msec(max.)
Package (Molded Package)			14-Pin DIP				Larger 8-Pin DIP	8-Pin DIP		Larger 8-Pin DIP	8-Pin DIP	14-Pin DIP	

64-Stage MN3003

128-Stage MN3006
256-Stage MN3009
1024-Stage MN3007

512-Stage MN3004
MN3002

*Pin connections for MN3002

Dual 512-Stage MN3010
MN3001

2048-Stage MN3008
4096-Stage MN3005

*Pin connections for MN3001

The device specification are subject to change without priornotice.

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